transistors being formed in a direction along a ~~<100>~~ crystal axis, or an axis equivalent to the ~~<100>~~ crystal axis,

the transistors including a plurality of n-channel field-effect ~~transistor~~ transistors and a plurality of p-channel field-effect ~~transistor~~ transistors, and

a trench width of the element isolating regions adjacent to regions at which the p-channel field-effect transistors are formed is narrower than a trench width of the element isolating regions adjacent to the n-channel field-effect transistors.

11. (original) The semiconductor device of claim 10, wherein the trench width of the element isolating regions that are adjacent to regions at which the p-channel field-effect transistors are formed and positioned in directions parallel and orthogonal to the direction joining the source and the drain is narrower than the trench width of the element isolating regions that are adjacent to regions at which the n-channel field-effect transistors are formed and positioned in directions parallel and orthogonal to the direction joining the source and the drain.

12. (original) The semiconductor device of claims 1 to 11, wherein the Raman shift of Raman spectrometry when a laser is irradiated onto channel portions of the n-channel field-effect transistors is smaller than the Raman shift of Raman spectrometry when a laser is irradiated onto channel portions of the p-channel field-effect transistors.

13. (original) The semiconductor device of claims 1 to 11, wherein the insulating film includes silicon nitride as a main component.

14. (currently amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

forming, on a semiconductor substrate, n-channel field-effect transistors and p-channel field-effect transistors disposed with a gate electrode and a drain and a source corresponding to the gate electrode;

depositing a stress control film so as to cover the field-effect transistors;

depositing and patterning a mask above the stress control film;

etching the stress control film;

depositing an interlayer insulating film after depositing the stress control film; and

forming, above the interlayer insulating film, a wiring layer that electrically communicates with the transistors,

wherein a direction that joins the source and the drain is formed in a direction along a ~~<100>~~ crystal axis or an axis equivalent to the ~~<100>~~ crystal axis,

~~tensility~~ tensile or compression strain is made to reside in the stress control film, and channel portions of the p-channel field-effect transistors in directions parallel and orthogonal to the direction joining the source and the drain are formed so as to include compression strain that is larger than that of channel portions of the n-channel field-effect transistors in directions parallel and orthogonal to the direction joining the source and the drain.

15. (original) The method of manufacturing a semiconductor device of claim 14, wherein the etching removes the stress control film from regions forming contact plugs and removes or makes at peripheries of the p-channel field-effect transistors the stress control film thinner than peripheries of the n-channel field-effect transistors.

16. (currently amended) A semiconductor device including a semiconductor substrate, a gate electrode and a plurality of ~~transistor~~ transistors formed on the semiconductor substrate, the transistors being disposed with a drain and a source corresponding to the gate electrode, and a plurality of ~~circuit~~ circuits disposed with the transistors,

wherein a first circuit is disposed with a first transistor and a second circuit is disposed with a second transistor,

a direction joining a corresponding drain and a source configuring the first transistor of the first circuit is formed in a direction along a ~~<100>~~ crystal axis of the substrate or an axis equivalent to the ~~<100>~~ crystal axis, and

a direction joining a corresponding drain and a source configuring the second transistor of the second circuit is formed in a direction along the ~~<100>~~ crystal axis of the substrate or an axis equivalent to the ~~<100>~~ crystal axis.